

ABSTRACT

A phase/frequency comparator is described which includes two edge-triggered storage elements, each set by
5 an edge of a reference frequency signal of a phase- or frequency-locked loop (PLL) and by an edge of an output frequency signal of the PLL. The storage elements are each reset by an output signal of a resetting logic unit, which is activated when both output signals of the storage
10 elements are activated and then deactivated when the output signals are deactivated.